IN THE CLAIMS

Please amend the claims as follows:

1. - 42. (Canceled)

43. (Currently Amended) A timing circuit, comprising:

~~an~~ a first input adapted to receive at least one first input signal, the ~~at least one~~ first input signal including a sense amplifier isolation signal adapted to isolate a first memory array; ~~and~~

a second input adapted to receive at least one second input signal, the second input signal including a sense amplifier isolation signal adapted to isolate a second memory array;

~~an~~ a first output connected to ~~an~~ a first address decoder adapted to address ~~a~~ the second memory array[[,]] ;

a second output connected to a second address decoder adapted to address the first memory array; and

wherein the timing circuit is adapted to selectively activate ~~activates~~ the second address decoder based on the ~~at least one~~ second input signal and the first address decoder based on the first input signal.

44. (Currently Amended) The timing circuit according to claim 43, wherein the ~~at least one~~ first input signal includes a RAS* signal.

45. (Currently Amended) The timing circuit according to claim 44, wherein the first output activates the first address decoder based on a low RAS* signal and a low isolation signal.

46. (Currently Amended) A timing circuit, comprising:

~~an~~ a first input adapted to receive at least one first input signal, the ~~at least one~~ first input signal including a first sense amplifier isolation signal;

a second input adapted to receive at least one second input signal, the second input signal including a second sense amplifier isolation signal;

~~an~~ a first output connected to ~~an~~ a first address decoder[[,]] ;

a second output connected to a second address decoder;

wherein the timing circuit is adapted to activate the first address decoder based on the first input signal; and

wherein the second isolation signal is associated to ~~the~~ a first memory array separate from a second memory array ~~connected to the address decoder~~, wherein the first isolation signal is associated to the second memory array.

47. (Currently Amended) The timing circuit according to claim 43, wherein the first input is connected to a NOR gate.

48. (Currently Amended) The timing circuit according to claim 43, wherein the first input is connected to an AND gate.

49. (Currently Amended) A timing circuit connected to a first wordline decoder of a first memory array and a second wordline decoder of a second memory array, the timing circuit comprising:

~~an~~ a first input adapted to receive at least one first input signal, the ~~at least one~~ first input signal including a sense amplifier isolation signal connected to a sense amplifier for ~~a~~ the second memory array; ~~and~~

~~an~~ a first output connected to the first wordline decoder, wherein the timing circuit is adapted to activate ~~activates~~ the first wordline decoder based on the ~~at least one~~ first input signal;

a second input adapted to receive at least one second input signal, the second input signal including a sense amplifier isolation signal connected to a sense amplifier for the first memory array; and

a second output connected to the second wordline decoder, wherein the timing circuit is adapted to activate the second wordline decoder based on the second input signal.

50. (Currently Amended) The timing circuit according to claim 49, wherein the ~~at least one~~ first input signal includes a RAS* signal.

51. (Currently Amended) The timing circuit according to claim 50, wherein the first output activates the first wordline decoder based on a low RAS* signal and a low isolation signal.

52. (Currently Amended) The timing circuit according to claim 49, wherein the first input is connected to a NOR gate.

53. (Currently Amended) The timing circuit according to claim 49, wherein the first input is connected to an AND gate.

54. (Original) The timing circuit according to claim 49, wherein the first memory and the second memory array are connected to one sense amplifier.

55.-69. (Canceled)

70. (Currently Amended) An integrated circuit, comprising:

a memory array,

a plurality of sense amplifiers operably connected to the memory array,

an isolation gate system operably connected between the memory array and the sense amplifiers, ~~and~~

a first timing ~~circuits~~ circuit operably connected to the isolation gate system, comprising:

~~an~~ a first input adapted to receive at least one first input signal, the ~~at least one~~ first input signal including a first sense amplifier isolation signal; ~~and~~

~~an~~ a first output operably connected to an address decoder and the first input, wherein the first timing circuit activates the address decoder for a first sub-array of the memory array based on the ~~at least one~~ first input signal; and

a second timing circuit operably connected to the isolation gate system, comprising:

a second input adapted to receive at least one second input signal, the second input signal including a second sense amplifier isolation signal; and

a second output operably connected to an address decoder and the second input, wherein the second timing circuit activates the address decoder for a second sub-array of the memory array based on the second input signal.

71.-88. (Canceled)

89. (Currently Amended) The timing circuit according to claim 46, wherein the ~~at least one~~ first input signal includes a RAS* signal.

90. (Currently Amended) The timing circuit according to claim 46, wherein the first output activates the address decoder based on a low RAS* signal and a low isolation signal.

91. (Currently Amended) The timing circuit according to claim 46, wherein the first input is connected to a NOR gate.

92. (Currently Amended) The timing circuit according to claim 46, wherein the first input is connected to an AND gate.

93. (Previously Presented) The timing circuit of claim 43, wherein the output is adapted to be connected to a wordline decoder of the address decoder.

94. (Previously Presented) The timing circuit of claim 70, wherein the output is adapted to be connected to a wordline decoder of the address decoder.

95. (New) The timing circuit according to claim 44, wherein the second input signal includes a RAS* signal.

96. (New) The timing circuit according to claim 95, wherein the second output activates the second address decoder based on a low RAS* signal and a low isolation signal.

97. (New) The timing circuit according to claim 47, wherein the second input is connected to a NOR gate.

98. (New) The timing circuit according to claim 48, wherein the second input is connected to an AND gate.

99. (New) The timing circuit according to claim 50, wherein the second input signal includes a RAS* signal.

100. (New) The timing circuit according to claim 99, wherein the second output activates the second wordline decoder based on a low RAS* signal and a low isolation signal.

101. (New) The timing circuit according to claim 52, wherein the second input is connected to a NOR gate.

102. (New) The timing circuit according to claim 52, wherein the second input is connected to an AND gate.